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Short startup, batteryless, self-starting thermal energy harvesting chip working in full clock cycle

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Abstract: The Internet of Things paradigm considers the deployment in the environment of a profusion of heterogeneous sensor nodes, connected in a complex network, and autonomously powered. Energy harvesting is the common proposed solution to supply such sensors, and many different sources such as light, mechanical vibrations, temperature differences can be considered individually or in combination. Specifically, a thermoelectric generator (TEG), taking advantage of the Seebeck effect, is able to harvest electrical power from a temperature gradient of a few degrees. This study presents a chip fabricated in 130 nm CMOS technology, designed to convert a typical 50 mV output from a TEG into 1 V. The batteryless design utilises both halves of a 50% duty cycle clock. Measurements have been performed by using a TEG, and an equivalent TEG model, i.e. voltage source (50 mV–200 mV) with a series resistance of 5 Ω. The result shows that the proposed prototype can extract 60% (at 50 mV) to 65% (at 200 mV) of the total available power. The energy harvester can self-start at 50 mV with a 2.8 ms startup time, which is a significant improvement over the past work.

1 Introduction

Thermal gradients exist in almost every environment and can be converted into usable electrical form used by humans in their daily life [1]. The thermoelectric generator (TEG) is one of the most suitable transducer for energy harvesting owing to its low cost and robustness [2]. These transducers have low open circuit voltage; however, sufficient available power for harvesting purposes [3]. The harvested power can be efficiently used by employing, a DC–DC converter to elevate the low-voltage generated by the TEG, to an appropriate voltage level at the load side. These DC–DC converters can be self-starting or it can be started by external means. A DC–DC converter can be used to power electronic circuits in a wearable devices, sensors node, often they can be used as a battery chargers etc.

A simplest self-starting DC–DC converter can be designed by using an oscillator coupled with a charge pump [4], the converter startup from 90 mV with a peak efficiency of 17%. A transformer-based discrete DC–DC converter is reported in [5], which can start from 60 mV and attains an efficiency of 72%. In [6], a 73% peak efficiency self-starting converter is reported, with a startup time >15 ms at 50 mV input. The work needs careful selection of the auxiliary inductor otherwise, the system can suffer from startup failure. A maximum peak power tracking-based harvesting system with 65% peak efficiency, which starts at 300 mV is reported in [7]. Bautista *et al*. [8], propose an energy harvester for multi-array TEGs; however, uses an external pre-charge voltage of 900 mV at the output capacitor for start-up and can give a peak efficiency of 61.1%. Converter reported in [9] starts from 100 mV and achieve an efficiency of 83.4%, providing an output voltage of 500 mV. A converter circuit for TEG with high-internal resistance is proposed in [10], it can self-start from 220 mV with 76% peak efficiency. Hernandez and Noije [11] report a fully integrated DC–DC converter, including inductors; however, can achieve an efficiency of 39% with 300 mV start-up, owing to the poor quality factor of on-chip inductors. An RF-based kick start TEG energy harvester has been reported in [12]. It uses an adaptive maximum power point tracking for TEG internal impedance matching, and simulation results shows that it can start from 50 mV with 65% peak efficiency. Recent work in [13–15], report energy harvesting prototypes with efficiency of 80, 57, and 58%, respectively, meant to harvest energy from different energy sources, with different startup voltage and startup time. Therefore, self-starting voltage, startup time and efficiency of the converter circuit can be identified area of research.

This paper will present the design and measurement results of a converter prototype fabricated in 130 nm CMOS technology that can extract more than 50% of the maximum available power from a TEG [16]. In the present circuit, the startup is fully electric and integrated (except inductors), and it can provide a regulated output. The converter prototype utilises both half cycles of the 50% duty clock, and uses zero current switching (ZCS) technique to open and close the P-channel metal oxide semiconductor (PMOS) switches; this help to achieve a peak efficiency of 65% by this converter circuit. Measurement results confirm good improvement in the circuit startup time over work reported in literature. The novelty of this work includes dual power path structure to increase the efficiency, and integrating enhanced swing ring oscillator (ESRO) to improve the converter start-up time. The work also proposes a novel circuit design for the ZCS and control logic scheme to generate complementary clocks, and also current starved delay circuit to minimise power consumption.

The paper is organised as follows. Section 2 presents the overall system. Section 3 discusses about sizing the inductors for the main and auxiliary stage. Section 4 presents details on the oscillator and the charge pump employed for start-up of the converter. Section 5 discusses about the peripheral circuits, namely: current starved oscillators, zero-current-switching circuit, control logic and reference voltage generator with voltage monitors. Section 6 presents the measurement results, and finally Section 7 presents conclusion along with scope of future work is drawn.

2 Overall system

The overall architecture of the circuit is shown in Fig. 1. The TEG is modelled by a low-voltage source V_{TEG} and a series resistance R_{TEG}. The auxiliary converter (L_{AUX}) is driven by a low-voltage starter (LVS). The LVS consists of a two-stage ESRO [17], and a 12-stage Dickson charge pump (DCP) [18]. The ESRO is potentially able to startup at around 30 mV in a fully integrated 130 nm CMOS technology. The DCP converts AC swing into a DC-voltage ($V_{\mathrm{O,\ DCP}}$), to power the first current starved ring

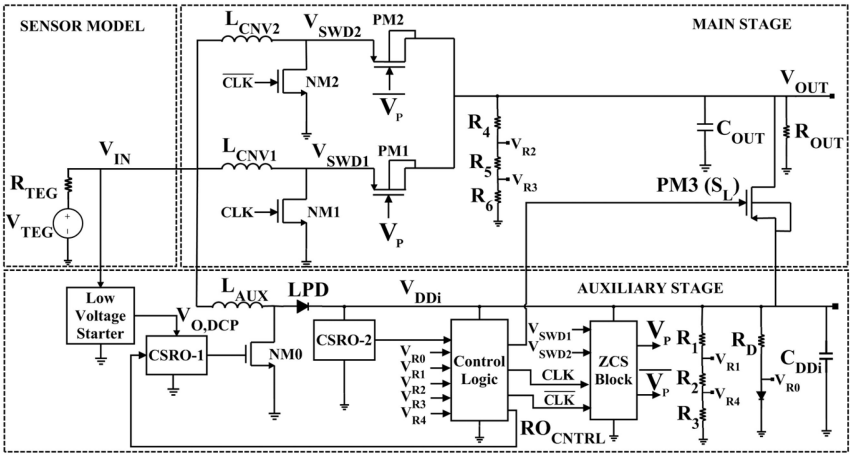


Fig. 1 *Simplified block diagram of the circuit along with essential blocks. NM-0, 1, 2 are the LVT NMOS switches and PM-1, 2, 3 are the LVT PMOS switches. RO_{CNTRL} is the disable signal for CSRO-1 when $V_{DDi} > 1$ V*

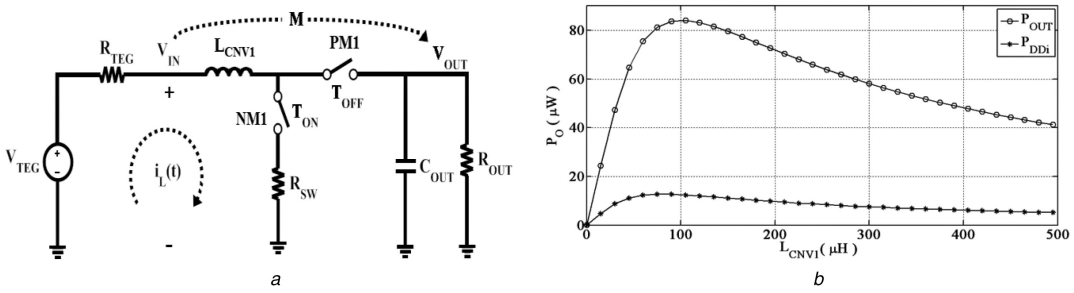


Fig. 2 *Derivation proof by using topology*

(a) V_{IN} is boosted by a factor M at the output V_{OUT} using switches NM1 and PM1. Output capacitor C_{OUT} is used to store charge, R_{OUT} is the load resistance, and R_{SW} is the switch resistance of NM1, ***(b)*** Extracted power by the main and auxiliary stage with different values of the inductors. This figure is plotted using (6) and dependent on switching time period T_{SW}, source power and internal impedance R_{TEG}. T_{SW} for main and auxiliary stage is taken as 10 and 40 μs, respectively

oscillator (CSRO-1). For $V_{O,\,DCP} = 500$ mV, the CSRO-1 oscillates with a time period of 10 μs. CSRO-1 drives an auxiliary boost converter stage, and consists of a low Vt (LVT) N-channel metal oxide semiconductor (NMOS) switch NM0, a LVT on-chip diode connected NMOS (LPD), and an off-chip inductor L_{AUX}.

The L_{AUX} boosts the voltage at V_{DDi} to 600 mV. Because of power consumption by the blocks connected to V_{DDi} node, an auxiliary boost converter has to be considered; otherwise connecting $V_{O,\,DCP}$ directly to the V_{DDi} will increase the minimum voltage to start the overall system. Connected to the V_{DDi} node is an on-chip capacitor of 1 nF. With this capacitor value, the peak-to-peak ripple at V_{DDi} is around 40 mV. Once V_{DDi} reaches 600 mV, the blocks connected to V_{DDi} node starts to work; all blocks consume a total current of 1.5 μA at 600 mV and 4 μA at 1 V.

The second CSRO-2 (CSRO-2) provides a clock of 40 μs at 600 mV for the control logic circuit, which in turn generates complementary clocks to drive the LVT switches NM-1, 2. A ZCS block generates complementary pulses to close and open the LVT PMOS switches PM-1, 2. The ZCS block consists of a delay block that generate 16 delays to cover the 50–200 mV range of the TEG voltage. A sequential search algorithm was used to choose one of the delays, according to the rising or falling edge of the V_{SWD1}/V_{SWD2} polarity, with respect to, $V_P/\overline{V_P}$ [6]. When V_{OUT} reaches to 600 mV, a LVT switch S_L closes to allow charge sharing between the V_{DDi} and V_{OUT} node, further boosting to 1 V. In this work, the inductors, L_{CNV1} and L_{CNV2} are energised separately for two half cycles of the clock pulse [16]. Using this technique, it is possible to extract more than 50% of the maximum available power from the TEG, and lower the ripple at the load for a given load capacitor value. Reference voltages generated from nodes V_{DDi} and V_{OUT}, along with control logic circuit helps in voltage monitoring and voltage regulation.

In [19], a zero order model/approximation is derived to show the power that can be extracted from the source. Derivation proves that by using topology shown in Fig. 2*a* and with a 50% duty cycle, it is possible to extract a maximum of 37.5% of the available power in one half cycle. If both half cycles are used, as proposed in this work, the maximum output power that can be extracted is 75% of the available power.

3 Main and auxiliary converters

This section will present a mathematical equation, to size the main and auxiliary stage inductors, $L_{CNV1,\,2}$ and L_{AUX}. Consider in Fig. 2*a* that a current i_L flows, when switch NM1 is closed. Practically the i_L current after considering boundary conditions can be expressed as

$$i_L(t) = \frac{V_{TEG}}{R_{SW} + R_{TEG} + R_{CNV1}}\left(1 - \exp\left(-\frac{t(R_{SW} + R_{TEG} + R_{CNV1})}{L_{CNV1}}\right)\right). \tag{1}$$

In (1), the peak value of current (I_P) will occur at $t = T_{ON}$, R_{CNV1} is the internal resistance of the inductor L_{CNV1}, and R_{SW} is the resistance of the switch NM1. The boost factor M ($=V_{OUT}/V_{IN}$) is related to I_O (load current) [20] as

$$M = 1 + \frac{V_{IN} D_1^2 T_{SW}}{2I_O \cdot L_{CNV1}}. \tag{2}$$

The average value of current I_O through PM1 can be expressed as

$$I_O = \frac{T_{OFF} I_P}{2T_{SW}} = \frac{D_1 \cdot I_P}{2(M-1)}. \tag{3}$$

In (3), $(M-1) = T_{ON}/T_{OFF}$ [20]. The duty cycle 'D_1' in (3) can be substituted in (2), to express I_O as

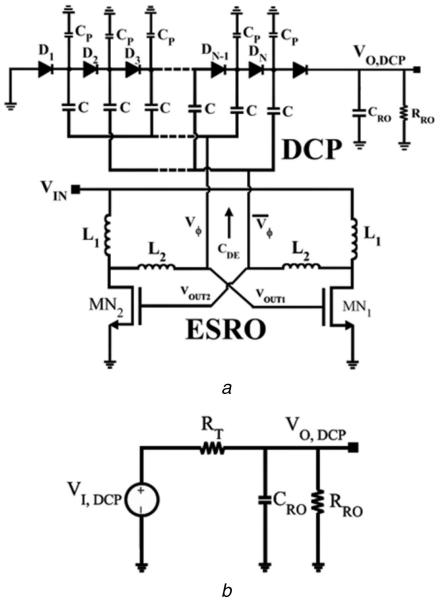


Fig. 3 *Low-voltage starter – ESRO coupled with DCP*

(a) In ESRO; L_1 and L_2 are off the shelf components. In DCP; C_{DE} is the equivalent capacitance presented by charge pump, and C and C_P are coupling and parasitic capacitance, respectively. V_ϕ and $\overline{V_\phi}$ are the peak voltage of the alternating signal and are complementary of each other, ***(b)*** In the equivalent model of DCP; $V_{I,\,DCP}$ is the voltage equivalent and R_T is the internal resistance of the charge pump. And C_{RO} and R_{RO} are the equivalent capacitance and the resistance of the CSRO-1, respectively. An on-chip diode with $V_T = 0.7$ V is integrated at $V_{O,\,DCP}$ node to protect the CSRO-1 from overvoltage

$$I_O = \frac{I_P^2 \cdot L_{CNV1}}{2(M-1)V_{IN}T_{SW}}. \tag{4}$$

In case of high gain, $M >> 1$, therefore, $M - 1 \cong M$; whereas the available output power (P_O) to the load is $I_O \times V_{OUT}$. Then it is possible to express (4) as

$$P_O \simeq \frac{I_P^2 \cdot L_{CNV1}}{2 \cdot T_{SW}}. \tag{5}$$

In (5), the I_P can be substituted by i_L ($t = T_{ON}$) given in (1), to express P_O as

$$P_O \simeq \left(\frac{V_{TEG}}{R_{EQ}}\right)^2\left(1 - \exp\left(-\frac{T_{ON}R_{EQ}}{L_{CNV1}}\right)\right)^2 \frac{L_{CNV1}}{2 \cdot T_{SW}}, \tag{6}$$

where in (6), $R_{EQ} = R_{SW} + R_{CNV1} + R_{TEG}$. Equation (6) is the P_O obtained from one half of the cycle (T_{ON}), and it should be multiplied by 2, when the inductors are energised for both halves of a 50% duty cycle clock.

The *W*/*L* (μm/μm) of the switches present in the auxiliary and main stage are as follows; NM0: (48 × 4)/0.48, NM1, 2: (480 × 4)/0.12, PM1, 2: (120 × 4)/0.12, and PM3: (3 × 4)/0.12. There are trade-offs in choosing the aspect ratio of the NM1, two switches, because a lower value will give higher conduction losses; and a larger value can increase the dynamic power (P_{dyn}), and static power (P_{stat}) loss related to sub-threshold current leakage, when switches are OFF. At $V_{DD} = 1$ V, the NM1, two switches has $P_{dyn} = 57.12$ nW, and $P_{Stat} = 2.52$ μW, this is acceptable considering the power budget of the circuit.

Equation (6) is used to select the value of inductors for the main stage and the auxiliary stage. The time period of CSRO-1 is 10 μs at 0.5 V, and time period of CSRO-2 is 40 μs at 0.6 V. The time period of CSRO-2 is larger than CSRO-1, to avoid losses during ZCS. The other parameters in (6) are: $V_{TEG} = 50$ mV, $R_{TEG} = 5$ Ω, $R_{CNV1} = 0.6$ Ω (assumed), R_{SW} (NM0) at 0.5 $V = 15$ Ω, and R_{SW} (NM1, 2) at 1 V = 0.45 Ω. In the auxiliary stage the LPD diode has a forward voltage drop $V_{DF} \cong 0.2$ V at peak current. In Fig. 2*b*, P_{OUT} and P_{DDi} is the power available to the load and blocks, respectively. From this figure, it can be observed that, in order to extract the maximum power, two 100 μH inductors should be used in the main stage. Since the R_{TEG} and T_{SW} do not change during circuit operation, the maximum efficiency for this topology is achieved, once L_{CNV1} is optimised by (6). It is worth noting that the losses in the inductors and switches reduces the maximum power extracted from 75 to 68% (85 μW of peak power for $V_{TEG} = 50$ mV). For auxiliary stage, any inductor from 100 to 500 μH, will be sufficient to power the peripheral. Next section will discuss in detail about the low-voltage starter block comprising of ESRO and DCP.

4 Low-voltage starter for AC–DC conversion

Low-voltage starter consists of ESRO coupled with DCP, as shown in Fig. 3*a*. ESRO is chosen because it can start to oscillate from a very low voltage with a swing greater than V_{IN}; voltage swings of various oscillators are analysed in [21]. This makes the ESRO, a convenient choice in driving a poorly efficient on-chip DCP powering the CSRO-1. In Fig. 3*a*, the ESRO has two large aspect ratio, zero Vt (ZVT) transistors, MN_1 and MN_2. L_1 and L_2 are external inductors with internal resistance R_1 and R_2, respectively. In Fig. 3*a* the capacitance (C_2) seen by the gates of $MN_{1,\,2}$ transistors is $C_2 = MN_{1,\,2}$ gate capacitance + C_{DE}. Let g_m, g_{ms} and g_{md} be the gate, source and drain transconductance of ZVT transistors $MN_{1,\,2}$. Let L_P and R_P be the parallel equivalent of L_1 and R_1, respectively.

The small signal transfer function for the ESRO is given by

$$\begin{aligned}\frac{V_{OUT1}}{V_{OUT2}} &= -\frac{g_m}{sC_2 + (G_P - jX_P)\cdot(A_0 + jB_0)} \\ &= -\frac{g_m}{G_PA_0 + X_PB_0 + j(\omega C_2 + B_0G_P - X_PA_0)}.\end{aligned} \tag{7}$$

In transfer function (7), $A_0 = 1 - L_2C_2\omega^2$; $B_0 = \omega C_2R_2$; $G_P = g_{md} + (1/R_P)$; $X_P = 1/\omega L_P$. When imaginary part of (7) is equated to zero, the oscillation frequency of ESRO will be

$$\omega_0 = \frac{1}{\sqrt{L_2C_2 + L_PC_2(1 + R_2G_P)}}. \tag{8}$$

In (8), $L_P \cong L_1$ and $R_2G_P << 1$ for high-Q inductors therefore ESRO oscillation frequency can be expressed as

$$f_0 = \frac{1}{2\pi\sqrt{C_2L_1(K+1)}}, \tag{9}$$

where, $K = L_2/L_1$. Oscillation in ESRO will happen when g_m is greater than the real part of the transfer function (7). On solving, condition (10) can be derived

$$\frac{g_{ms}}{g_{md}} - \left(1 + n\left[\left(1 + \frac{1}{g_{md}R_P}\right)\frac{1}{K+1}\right] + \frac{C_2R_2}{g_{md}L_1}\right) > 0. \tag{10}$$

In (10), $R_P = \omega_0 \cdot Q_1 \cdot L_1$, where Q_1 is L_1 quality factor, and n is the transistor slope factor. In (10), it is worth noting that the value of C_2 is in pF and g_{md} is in mA/V, therefore $C_2 << g_{md}L_1$ irrespective of the R_2 value. Expression (10) is an approximate condition for the required g_{ms}/g_{md} ratio (voltage gain in the common-gate configuration), that can start oscillation in the ESRO [17].

Fig. 3*a* also shows the diagram of a Dickson-based voltage multiplier [18], in which the diode is a gate to source connected ZVT transistor with $W/L = 4/0.42$ (μm/μm), and N is the number of multiplier stages. In the equivalent DCP shown by Fig. 3*b*, $V_{I,\,DCP}$ is given as

Table 1 Parameter along with their values for ESRO and DCP

Parameter	$MN_{1,2}$	N	C, pF	C_P, pF	I_S, μA	I_L @ 0.5 V	R_{RO}, MΩ	C_{RO}, pF
value	(6 × 40) × 4/0.42	12	6.4	0.5	3.2	66 nA	8	5

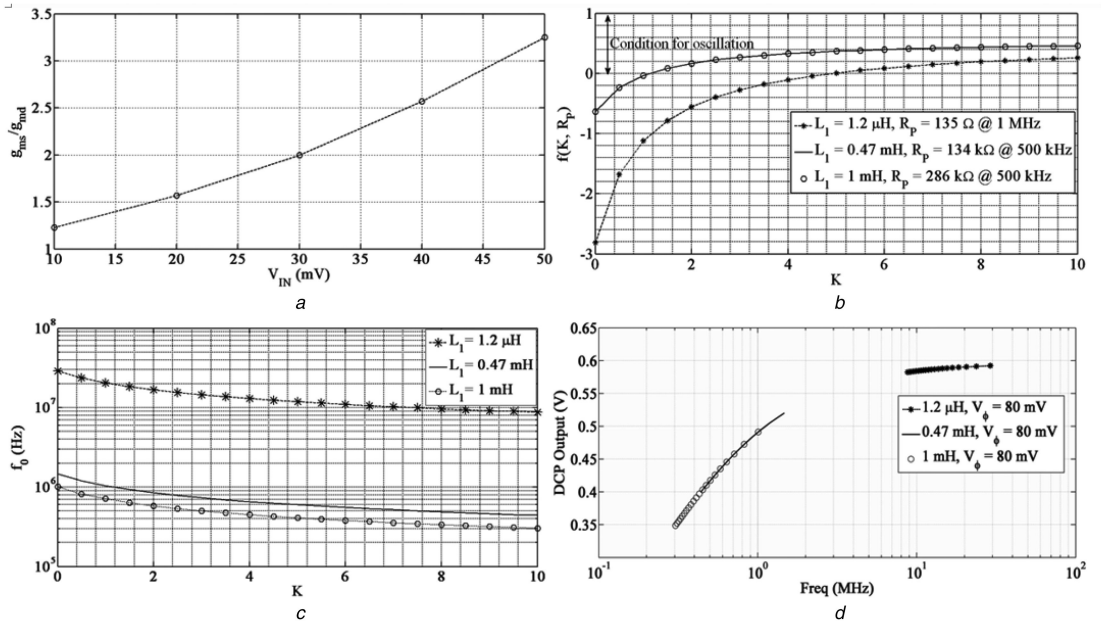


Fig. 4 *Quality factor of external inductors in ESRO affects the startup voltage and the peak to peak voltage swing*
(a) Plot of V_{IN} versus extracted g_{ms}/g_{md} ratio. The g_{ms} and g_{md} are extracted from a derivative of the output characteristics corresponding to the same gate, source and drain voltage. Note that increasing value of g_{ms}/g_{md} will increase chances of oscillation, because condition in (10) is strongly satisfied, ***(b)*** Function $f(K, R_P)$ represents the left hand side of (10). Plot shows that with inductor 0.47 and 1 mH, oscillation is more likely than 1.2 μH, for the greater value of K, ***(c)*** Oscillation frequency versus $K = L_2/L_1$. In this plot the estimated value of $C_2 = C_{DE} + C_{gate}(MN_{1,2}) = 25$ pF, ***(d)*** Plot shows that the charge pump output drops when oscillation frequency decreases. The charge pump output on the large extent depends upon the peak voltage swing V_ϕ from ESRO

$$V_{I,DCP} = N \cdot \left[\frac{C \cdot V_\phi}{C + C_P}\right] - (N+1) \cdot n \cdot U_T \ln\left[2\left(1 + \frac{I_L}{I_S}\right)\right], \quad (11)$$

In (11), diode forward voltage drop is replaced by load current I_L and saturation current I_S. The R_T in Fig. 3*b* is given as

$$R_T = N\left[\frac{1}{(C + C_P)f_0} + \frac{n \cdot U_T}{2I_S(1 + (I_L/I_S))}\right]. \quad (12)$$

In (11), and (12), $U_T = 26$ mV is the thermal voltage at 25°C. Net DCP output voltage, $V_{O,DCP}$ can be expressed as

$$V_{O,DCP} = \frac{R_{RO}}{R_T + R_{RO}} \cdot V_{I,DCP}. \quad (13)$$

The aspect ratio of the diode connected transistor is small, therefore C_{DE} can be closely approximated as

$$C_{DE} \simeq \frac{C + C_P}{2} \times \frac{N}{2}. \quad (14)$$

In (14), C is the coupling capacitor and C_P is the parasitic capacitance, usually $C >> C_P$. Equations (9)–(14) are used to minimise the value of the input voltage. The optimisation of ESRO coupled with DCP, is done by software simulation; such optimisation is discussed in [22]. The optimisation yields the parameter values given in Table 1. The extracted value of g_{md} for the aspect ratio of $MN_{1,2}$ mentioned in Table 1 remain close to 4.1 mA/V, for an input voltage range of 10–50 mV.

Fig. 4*a* shows a plot between the extracted value of g_{ms}/g_{md} versus for a ZVT transistor with $W/L = 4.2/0.42$ μm/μm. The quality factor of external inductors in ESRO affects the startup voltage and the peak to peak voltage swing; this will change the DCP output loaded by CSRO-1. Fig. 4*b* shows the plot of (10), for three values of the inductors. R_P for three different inductor values has been measured at 1 MHz and 500 kHz using an LCR metre. In Fig. 4*b* the value of g_{ms}/g_{md} is equal to 1.57, this corresponds to 20 mV supply voltage (according to Fig. 4*a*). Fig. 4*b* shows that the large value inductor is more likely to oscillate than small value inductor, because it strongly satisfies the condition given by (10). However, according to (9), large value inductor decreases the frequency of ESRO oscillation (f_0), this is shown in Fig. 4*c*.

In Fig. 4*d*, the DCP output is plotted for a frequency range of 100 kHz–100 MHz, for each of the three inductors. From Fig. 4*d*, it can be observed that DCP output falls with decreasing frequency, and minimum startup voltage can be achieved only with the large value inductor. This is a trade off in the ESRO coupled with DCP.

A voltage of 0.45 V at the output of DCP is sufficient to power the CSRO-1, driving an auxiliary inductor. Therefore, $L_1 = 0.47$ mH, and $K \cong 5$ is chosen for the ESRO. With these values, the oscillator can start to oscillate from 30 mV, and the overall circuit will start when input reaches 50 mV. Next section will briefly discuss the design of the peripheral circuits' essential in driving L_{AUX} and $L_{CNV1,2}$.

5 Peripheral circuits

The peripheral circuits consist of two CSROs, ZCS circuit, control logic and reference generator with node sensing network (voltage monitors). The careful design of these blocks is very important for power management; all blocks should consume small value of supply current, because it can affect the efficiency of the overall system. Moreover, voltage regulation is important because when the available power increases, a constant voltage has to be maintained on the load side.

5.1 Current starved ring oscillator-1, 2

The schematic of CSRO is shown in Fig. 5*a*, it consists of chain of ring oscillators and a bias current circuit, which contains a high-

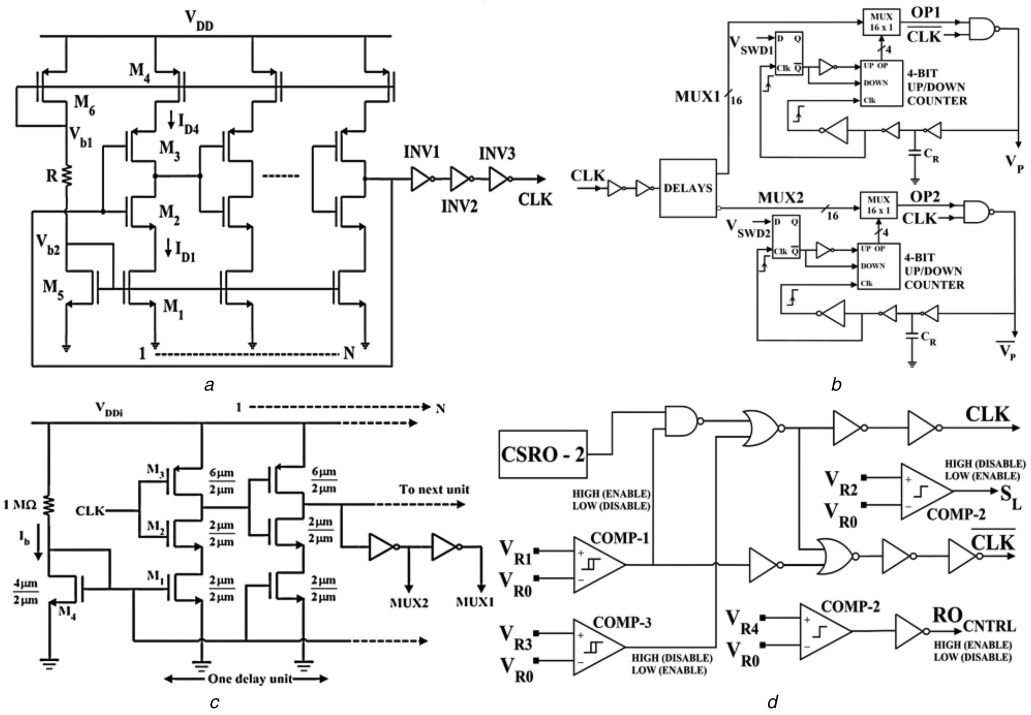


Fig. 5 *CSRO, ZCS and Control logic circuit* ***(a)*** *CSRO circuit schematic. The inverters: INV1, INV2 and INV3 are implemented with minimum width and length. R = 8 MΩ is a high-value on-chip resistance [23],* ***(b)*** *ZCS scheme to ON/OFF the switch PM1, 2,* ***(c)*** *Delay circuit, is implemented with Tox = 52 Å transistors. N = 16 is the number of such delay circuits,* ***(d)*** *Control logic block is responsible for voltage regulation and clocks generation*

Table 2 Transistors size in CSRO-1, 2. *W/L* is in (μm/μm)

W/L	M_6	M_5	M_4	M_3	M_2	M_1
1	4/4	4/4	4/4	4/2	2/2	4/4
2	4/4	4/4	4/4	8/4	4/4	4/4

value resistor R, to feed the oscillator. Table 2 shows the values of the aspect ratio used in the two oscillators.

5.2 ZCS network

The ZCS technique is used to open the PMOS switches, when the current through inductors $L_{CNV1,\ 2}$ reduces to zero. The ZCS problem and its solutions are widely discussed and reported in literature elsewhere [6–8]. The circuit shown in Fig. 5*b* implements ZCS for both the half cycles, based on the concept presented in [6]. A static D-flip flop is used to sense the change in the polarity of V_{SWD1} and V_{SWD2} at the rising edge of clock pulse V_P and $\overline{V_P}$. The D-flip flop runs a 4-bit counter to select one of the delay through the 16-line multiplexer. To cover 50–200 mV range, a delay range of 0.57–2.25 μs is selected. In the delay block, a current starved arrangement shown in Fig. 5*c* is used to limit power consumption. For a range of 50–200 mV, 4-bit will give a resolution of 10 mV, which is suitable for the present TEG. A logical NAND operation is performed with the main clocks CLK and $\overline{CLK}$, to shape the control pulse for PM1, 2 switches. Due to close circuit loop, the V_P and $\overline{V_P}$ is dynamically adjusted to a position till there is no change in the polarity of $V_{SWD1,\ 2}$. Simulation result shows that a delay of 1.5 ps (between $V_P/\overline{V_P}$ and V_{SWD1}/V_{SWD2}), will be sufficient to sense the change in polarity, at an appropriate instant of time. Therefore, in Fig. 5*b*, $C_R = 0.21$ pF and inverters have been used for 1.5 ps delay.

5.3 Control logic

The detailed circuit diagram of the control logic block is shown in Fig. 5*d*. The main function of this block is to generate complementary clocks, and to regulate voltage at the load end. The V_{DDi} and V_{OUT} nodes are checked for two voltages 0.6 and 1 V, by the reference circuit and the node sensing networks. Voltage comparators [23], working in weak inversion, enable or disable the gates, whenever the two voltage levels are reached. To keep the $V_{OUT} = 1$ V under different value of load resistance, a comparator-3 (Comp-3) with 100 mV hysteresis bandwidth [23], provides the gated regulation scheme to the load resistance. As shown by the flowchart in Fig. 6, comp-3 senses the load voltage; once the output voltage is charged up to be >1 V by V_{TC+}, the CSRO-2 is disabled through the gate. The load current is supplied by the C_{OUT} till the output voltage is discharged to be <1 V by $V_{TC-} = 50$ mV, and then CSRO-2 is enabled again.

5.4 Reference generator and sensing node

In the present design, simple voltage reference circuit less sensitive to process variation, is desirable. The circuit configuration shown in Fig. 7*d–a*, is used as reference generator. To sense V_{DDi} and V_{OUT} node voltages, the circuit configurations shown in Figs. 7*d–b* and *d–c*, are used. Fig. 7*e* shows the corner simulation waveform of the reference voltages with respect to node voltages, V_{DDi} and V_{OUT}. The figure shows that, V_{R0} (tt) = 0.26 V, and at the two extreme corners: V_{R0} (sf) = 0.28 V, V_{R0} (fs) = 0.24 V. This is acceptable in the present design. Next section will present the measurement results from the energy harvesting prototype.

6 Measurement results

Fig. 8*a*, shows the picture of the die realising the proposed circuit in 130 nm CMOS technology. The main circuit area is 0.8 mm × 0.82 mm. The area of the PCB is 5 cm × 6 cm and is shown in Fig. 8*b*. The prototype is in 28-pin DIP package. The efficiency of the converter circuit is measured by using a TEG from Tellurex (model G1-1.0-127-1.27), with sensitivity and internal resistance of 25 mV/K and 5 Ω, respectively. To measure the transient response

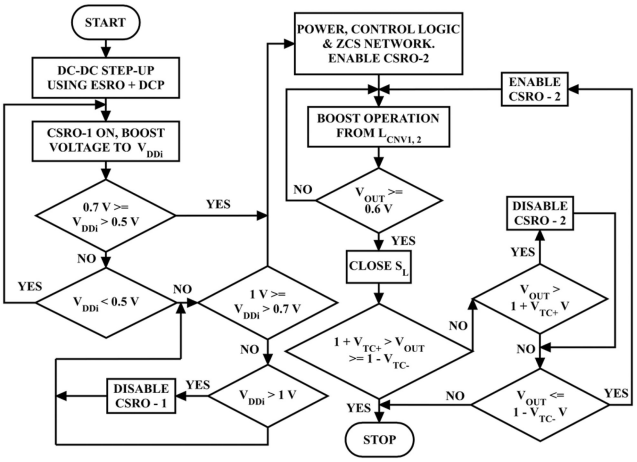


Fig. 6 *Flowchart to show the scheme of voltage regulation in the energy harvesting chip. VTC + = VTC − = 50 mV*

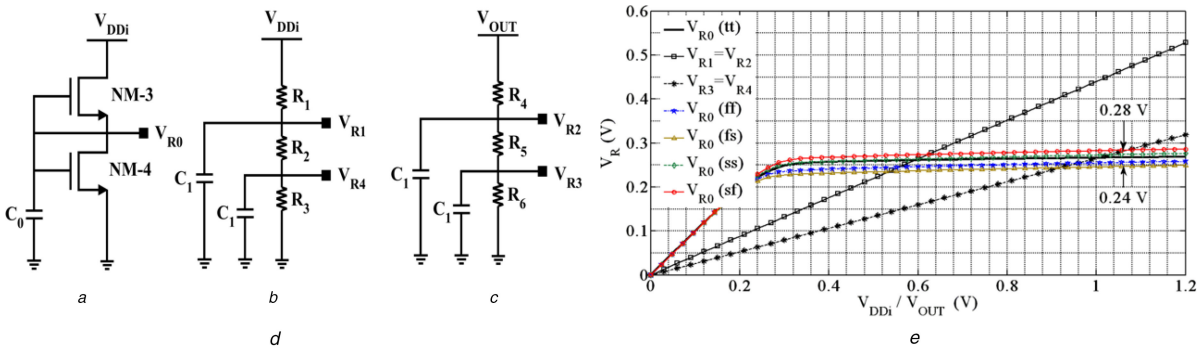


Fig. 7 *Circuit configurations for reference generation and corresponding corner simulation*

(d–a) NMOS devices based reference voltage generator, NM-3 is a LVT device with W/L = 3/1 (μm/μm), and NM-4 is a standard Vt device with W/L = 0.16/0.12 (μm/μm), C_0 = 2 pF, ***(d–b)*** Resistance ladder for sensing V_{DDi} node, ***(d–c)*** Resistance ladder for sensing V_{OUT} node, C_1 = 0.1 pF [23], ***(e)*** Plot of reference voltages with respect to voltages V_{DDi} and V_{OUT}. Magnitude of the resistors are in MΩ. Meaning of corners are: tt-typical typical; ff-fast fast; sf-slow fast; fs-fast slow, and ss-slow slow

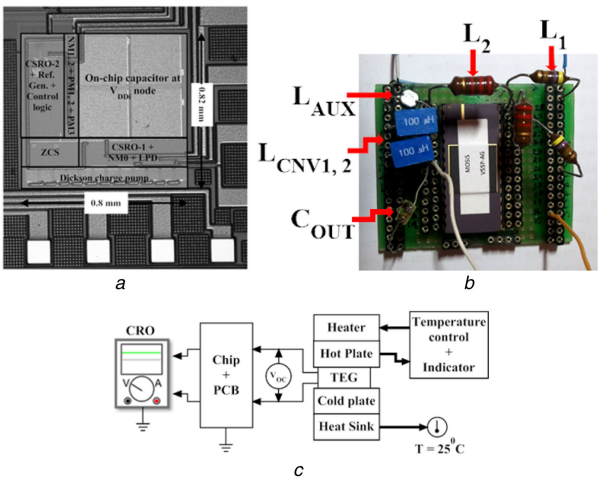


Fig. 8 *Picture of the die realising the proposed circuit in 130 nm CMOS technology*

(a) Photo of the die implementing the circuit shown in Fig. 1, ***(b)*** Photo of PCB for testing the prototype, ***(c)*** Measurement setup to measure power performance of the prototype, where T is the room temperature

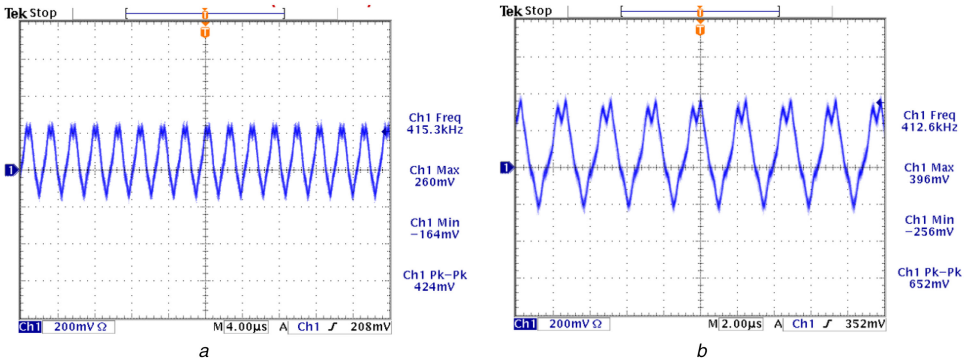
of the converter circuit, a source unit (HP® 3245A), and a 5 Ω resistance in series, is used to emulate the TEG model.

The values of the off-chip components used in the present work are: C_{OUT} = 100 nF, $L_{CNV1, 2}$ = 100 μH, L_{AUX} = 330 μH, ESRO: L_1 = 0.47 mH and L_2 = 2.2 mH. A 50 kΩ potentiometer (R_{OUT}) was connected to the output of the chip. On load side, the peak to peak ripple voltage is 50 mV with 100 nF output capacitor, considering T_{SW} (main stage/CSRO-2) = 42 μs at 1 V.

Fig. 8*c* shows the measurement setup used for the converter characterisation. With a constant temperature on the cold plate, the temperature of the hot plate is incrementally increased. The open circuit voltage is measured using a high-impedance multimetre (V_{OC}), to match the temperature difference with the open circuit voltage of this TEG. After taking readings, the multimetre is removed, wires to the PCB are connected, and the voltage at the load side is measured with an oscilloscope.

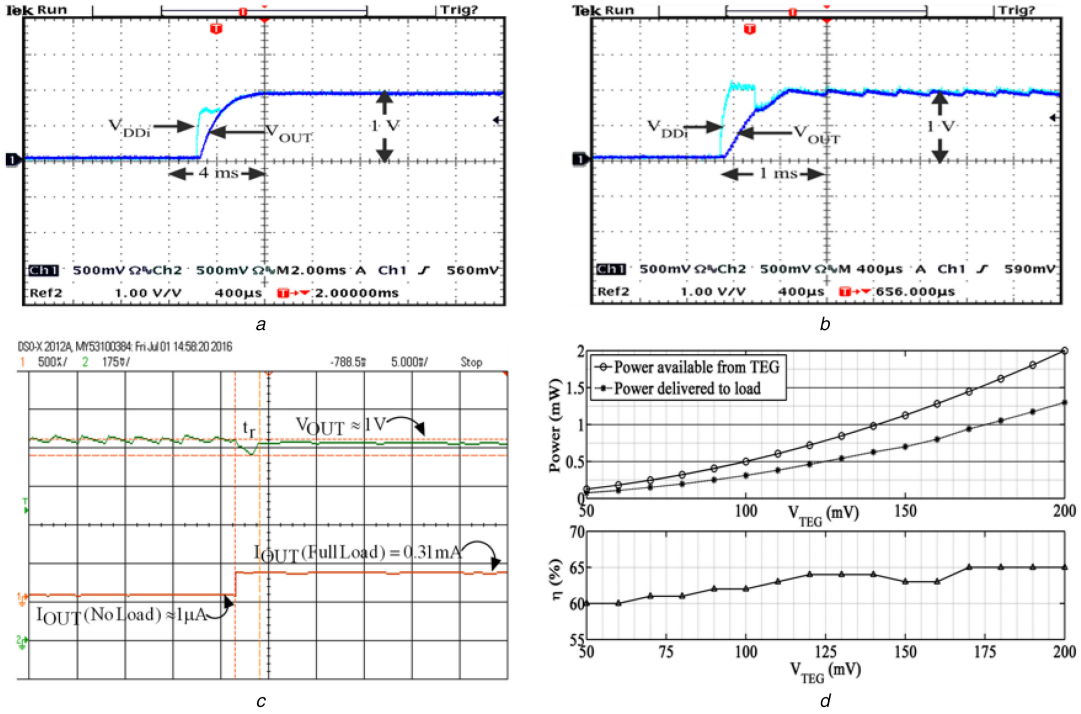
The efficiency η is herein defined as

$$\eta = \frac{P_{OUT}|_{V_{OUT}=1\,V}}{P_{AV}} \times 100\%, \tag{15}$$



a *b*

Fig. 9 *Measured ESRO oscillation for*
(a) $V_{TEG} = 30$ mV, ***(b)*** $V_{TEG} = 50$ mV



a *b* *c* *d*

Fig. 10 *Response of the chip*
(a) Measured waveforms of the voltages within the thermal harvesting circuit during startup from a 50 mV input voltage, ***(b)*** Measured waveforms of the voltages within the thermal harvesting circuit during startup from a 100 mV input voltage, shows the regulated output, ***(c)*** Load transient response for $V_{TEG} = 100$ mV, t_r is the load transient response time, ***(d)*** Diagram showing the available power and the extracted power from the TEG, same figure also shows the efficiency

where, $P_{AV} = V_{TEG}^2/4R_{TEG}$, and V_{OUT} is the voltage across the load which is around 1 V in this work. However, V_{OUT} is dependent on the reference generator susceptibility to process variation.

In the present circuit the auxiliary stage starts as soon the ESRO + DCP power the CSRO-1; this shortens the circuit transient settling time compared with [6]. Figs. 9*a* and *b* shows ESRO oscillation, 30 mV is the minimum voltage which will start ESRO only. 50 mV is the voltage which will start overall circuit to power up the load resistance. Figs. 10*a* and *b*, shows the measured waveform at the output, in response to an input voltage $V_{TEG} = 50$ and 100 mV. Fig. 10*a*, show the response of the chip when $V_{TEG} =$ 50 mV. It shows that the V_{DDi} and V_{OUT} closes at 600 mV and the output is boosted to 1 V. Current and power consumed by the low-voltage starter are 0.1 mA and 5 µW, respectively.

Fig. 10*b*, shows another response of the chip when $V_{TEG} = 100$ mV. In this figure the load is half of the maximum value with $V_{OUT} = 1$ V. The figure shows working of the gated regulation by the comparator threshold voltages V_{TC+} and V_{TC-}, which regulate the load voltage to an average value of 1 V. The maximum value of load obtained at 50 mV is 74 µA and at 100 mV is 0.31 mA.

Load transient measurement is performed to evaluate the converter performance [24]. Fig. 10*c* shows the transient response captured by the oscilloscope, when a load is connected through a switch. Ripple is observed at no load, then a transient time (t_r) of 2 ms is observed when switch is closed, after which converter stabilises to maintain a constant load voltage. Thus, Figs. 10*a–c*, show that the prototype chip is working according to the design specifications.

Fig. 10*d* shows the plot of measured extracted power from the available power, at different value of V_{TEG}. The V_{TEG} value represents a temperature difference of 2 to 8°K across the TEG surface. Same figure shows an efficiency which varies from 60 to 65% at 50 and 200 mV, respectively. These results are close enough with the derivation on the extraction of maximum power from available power in [19].

As derived from mathematical equations in [19], that in case of an ideal converter the maximum harvesting efficiency is 75%, for this type of architecture. The overall efficiency is decreased since there is the power loss due to non-ideal switches, non-ideal boost inductors, and peripheral circuits etc. Therefore, the difference between the ideal case and the measured results are acceptable.

An approximate power estimation using circuit simulation to match with the measurement result at 50 mV is presented here: total available power ≅125 µW (100%), measured power at load (extracted power) = 74 µW (≅60%), power loss because of inductor and switching resistance = 9 µW, converter circuit power

Table 3 Comparison of this work with some self-starting TEG energy harvester prototypes

Specification	[6]	[7]	[9]	[10]	[13][a]	[14][b]	[15]	This work
process, nm	65	180	180	65	180	180	130	130
startup voltage, mV	50	300	100	220	140	350	70	50
startup time	>15 ms	X	X	10.5 ms	>280 s	>60 s	1.5 s	<5 ms
efficiency, %	73 (peak)	65 (peak)	83.4 (peak)	76 (peak)	80 (peak)	57 (end to end)	58 (end to end)	65 (peak)
regulated output voltage	1.2 V	1.8 V	0.5 V	1.3 V	1 V	1.8 V	1.2 V	1 V
output power @ V_{TEG}	1.22 mW @ 200 mV	0.27 mW @ 300 mV	1 mW @ 100 mV	20.42 µW @ 220 mV	1 µW @ 620 mV	1 mW	17 µW @ 70 mV	1.3 mW @ 200 mV

[a]Intended to harvest energy from solar cell.

[b]Intended to harvest energy from TEG, photo voltaic cell and microbial fuel cell.

consumption = 4 µW, parasitic and switching power losses = 7 µW, total power lost = 20 µW.

During measurement, ten chips were tested and three chips were showing peak efficiency of 65%, two chips were showing the peak efficiency of 58%, and remaining five showed the peak efficiency in between these extremes.

Table 3 shows a comparison of this work with the recent available works. The main advantage of using a dual boost structure is the small value of ripple at the load side that can be obtained with a low value of the output capacitor, this reduces the device volume. However, it also results in disadvantage because it increases the inductor count by one, as SMD inductor is costly therefore overall cost increases.

7 Conclusion and scope of future work

In this paper an energy harvester for a TEG is presented; the prototype is fully integrated (excluding inductors and load capacitor) with self-starting capability. It can provide 1 V output with a peak efficiency of 65% and can startup in short time. The present work can be further improved by pushing startup to a lower voltage, i.e. 20–30 mV, as well by increasing the efficiency of the overall circuit. Moreover, a mechanism to turn off the low-voltage circuit can be implemented to save the circuit power consumption.

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